CLAIMS

1. A semiconductor structure comprising:

a substrate;

a lattice-mismatched first layer deposited on said substrate and annealed at a temperature greater than 100°C above the deposition temperature; and

a second layer deposited on said first layer with a greater lattice mismatch to said substrate than said first layer.

2. The semiconductor structure of claim 1, wherein said substrate comprises Si and said first and second layers comprise $Si_{1-x}Ge_x$.

3. The semiconductor structure of claim 1, wherein said substrate has a surface layer comprising Si and said first and second layers comprise $Si_{1-x}Ge_x$.

4. The semiconductor structure of claim 1, wherein said substrate comprises GaAs and said first and second layers comprise $In_yGa_{1-y}As$.

5. The semiconductor structure of claim 1, wherein said substrate has a surface layer comprising GaAs and said first and second layers comprise $In_yGa_{1-y}As$.

6. The semiconductor structure of claim 1, wherein said substrate comprises GaP and said first and second layers comprise $In_zGa_{1-z}P$.

7. The semiconductor structure of claim 1, wherein said substrate has a surface layer comprising GaP and said first and second layers comprise $In_zGa_{1-z}P$.

8. The semiconductor structure of claim 2, wherein said first and second layers differ by a Ge concentration less than 10% Ge.

9. The semiconductor structure of claim 2, wherein said first and second layers differ in Ge concentration by approximately 1.5% Ge.

10. The semiconductor structure of claim 2, wherein said first and second layers of $Si_{1-x}Ge_x$ are deposited at a growth temperature less than 850°C.

11. The semiconductor structure of claim 2, wherein said annealing occurs at a temperature greater than 900°C.

12. The semiconductor structure of claim 2, wherein anneal time is greater than 0.1 seconds.

13. The semiconductor structure of claim 2, wherein said first and second layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C.

14. The semiconductor structure of claim 2, wherein said first and second layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C, and the anneal time is greater than 0.1 seconds.

15. The semiconductor structure of claim 1, wherein said lattice-mismatched semiconductor layer is deposited by chemical vapor deposition.

16. A semiconductor graded composition layer structure on a semiconductor substrate comprising:

a semiconductor substrate;

a first semiconductor layer having a series of lattice-mismatched semiconductor layers deposited on said substrate and annealed at a temperature greater than 100°C above the deposition temperature;

a second semiconductor layer deposited on said first semiconductor layer with a greater lattice mismatch to said substrate than said first semiconductor layer, and annealed at a temperature greater than 100°C above the deposition temperature of said second semiconductor layer.

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17. The structure of claim 16, wherein said substrate comprises Si and said first and second layers comprise SiGe.

18. The structure of claim 16, wherein said substrate has a surface layer comprising Si

and said first and second layers comprise $Si_{1-x}Ge_x$.

19. The structure of claim 16, wherein said substrate comprises GaAs and said first and second layers comprise $In_yGa_{1-y}As$.

20. The structure of claim 16, wherein said substrate has a surface layer comprising GaAs and said first and second layers comprise $In_yGa_{1-y}As$.

21. The structure of claim 16, wherein said substrate comprises GaP and said first and second layers comprise $In_zGa_{1-z}P$.

22. The structure of claim 16, wherein said substrate has a surface layer comprising GaP and said first and second layers comprise $In_zGa_{1-z}P$.

23. The structure of claim 17, wherein sequential layers in the graded composition layers differ by a Ge concentration less than 10% Ge.

24. The structure of claim 17, wherein sequential layers in the graded composition layers differ in Ge concentration by approximately 1.5% Ge.

25. The structure of claim 17, wherein said first and second layers are deposited at a growth temperature of less than 850°C.

26. The structure of claim 17, wherein said annealing occurs at a temperature greater than 900°C.

27. The structure of claim 17, wherein anneal time is greater than 0.1 seconds.

28. The structure of claim 17, wherein sequential layers in the graded composition layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C.

29. The structure of claim 17, wherein sequential layers in the graded composition layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C, and the anneal time is greater than 0.1 seconds.

30. The semiconductor structure of claim 16, wherein said lattice-mismatched semiconductor layer is deposited by chemical vapor deposition.